SystemC Standardization Update Including UVM for SystemC

Accellera Systems Initiative SystemC Standards Update

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Presentation Overview

• Accellera Overview
  – Membership list
  – How to join a WG
  – Global SystemC events
• Number of IEEE-1666 standard downloads
• Accellera SystemC Working Group updates
  – Language & Transaction-Level Modeling
  – Configuration, Control & Inspection
  – Synthesis
  – Analog/Mixed-Signal
  – Verification
• Proposed Working Group information
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All Members Can Join SystemC WGs!

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Join A Working Group And Contribute!

Charter
This group is responsible for the definition of a synthesizable subset of SystemC.
Chair: Andres Takach, Mentor Graphics
Vice-Chair: Michael Meredith, Forte Design Systems

Background
In August 2009, this group released the Synthesis Subset Draft 1.3 standard synthesis subset draft for public review. The draft features several technical updates. Supported language constructs are now established, and a chapter on processes, clocks, and resets has been added. The draft also includes a discussion on abstraction levels that puts the concepts of the synthesizable subset in the context of the abstraction levels defined for TLM.

Public review of the draft is now closed. The draft is available for download here.

Join this Working Group
If you are an employee of a member company and would like to join this working group (requires login) and click Join Group. WG participation requires right of entry by the group chair.
SystemC Community

- Online at http://accellera.org/community/systemc
- Community forums, upload area for contributions, SystemC news
Global SystemC Presence 2014+

• **DVCon USA**  March in Silicon Valley
• **DAC**  June in San Francisco

**NEW**

• **DVCon India**  September in Bangalore
• **DVCon Europe**  October in Munich
• **SystemC Japan**  June 19, 2015
• **Accellera Day Taiwan**  1st half of 2015
IEEE 1666 SystemC Downloads


IEEE Computer Society

Sponsored by the
Design Automation Standards Committee

IEEE Std 1666™-2011
(Revision of
IEEE Std 1666-2005)

IEEE
3 Park Avenue
New York, NY 10016-5997
USA
9 January 2012

SystemC Overview

![Diagram of SystemC Overview]

Application
Written by the End User

Methodology- and Technology-specific Libraries

User Libraries

TLM
AMS
SCV
CCI

SystemC Core Language

Structural Elements
- Modules
- Ports
- Exports
- Interfaces
- Channels

Predefined Channels
- Signal, clock, FIFO, mutex, semaphore

Utilities
- Report handling, tracing

Data Types
- 4-valued logic type
- 4-valued logic vectors
- Bit vectors
- Finite-precision integers
- Limited-precision integers
- Fixed-point types

Event-driven Simulation
- Events, processes

Programming Language C++
ISO/IEC Std. 14882-2003

CCI standardization effort is underway

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Slide 8
March 2, 2015
SystemC Language & TLM WG

• **Charter:** Responsible for the definition and development of the SystemC core language, the foundation on which all other SystemC libraries and functionality are built.

• **Current status**
  – Maintenance release version 2.3.1 of the proof-of-concept simulator in April 2014 (bug fixes, experimental features)

• **Plans for 2014/2015**
  – Discuss new concepts affecting simulation performance
  – Collect, address, refine proposals and errata towards IEEE 1666-201x
SystemC 2.3.1 Maintenance Release

- Release of 2.3.1 in April 2014
  - Bug fixes for known issues wrt. IEEE 1666-2011
  - Some feature additions beyond IEEE 1666-2011 (may require explicit configuration during library build)
  - Code cleanups, deprecation of non-standard
Roadmap for IEEE 1666-201x

• Next IEEE 1666 update later this decade
  – Several errata and proposals already addressed in 2.3.1
  – Formal standardization will be moved to IEEE when sufficient input is available
• LWG/TLMWG are currently collecting proposals
  – Report your favorite missing feature/extension/annoyance
  – Non-Accellera members can use the community forums
• Parallelization of SystemC could be significant driver
  – More contributors needed!
SystemC Synthesis WG

• Charter: To define the SystemC synthesis subset to allow synthesis of digital hardware from high-level specifications.

• Current status
  – Releasing draft standard for 3-month public review
  – www.accellera.org/apps/org/workgroup/swg

• Plans for 2015
  – Process feedback from review in Q2 2015
  – Release standard in Q3 2015
  – Start work on new topics for the second version of the standard
Configuration, Control & Inspection WG

WG is defining these initial focus:

Goal: Standardizing interfaces between models and tools
SystemC Analog/Mixed-Signal WG

• **Charter:** The SystemC AMS Working Group is responsible for the standardization of the SystemC AMS extensions, defining and developing the language, methodology and class libraries for analog, mixed-signal and RF modeling in SystemC

• **Current status**
  – Released the SystemC AMS 2.0 standard in March 2013

• **Plans 2014/2015**
  – Publish User’s Guide update based on SystemC AMS 2.0
  – IEEE P1666.1 SystemC AMS Working Group started – Accellera contributed SystemC AMS standard to IEEE-SA
SystemC Verification WG

• **Charter:** The Verification Working Group (VWG) is responsible for defining verification extensions to the SystemC language standard, and to enrich the SystemC reference implementation by offering an add-on libraries (SystemC Verification (SCV) library, etc.) to ease the deployment of a verification methodology based on SystemC.

• **Current Status**
  – Released version 2.0 of SystemC Verification library (SCV) in April 2014

• **Plans for 2014/2015**
  – Integrate the UVM verification methodology in SystemC
  – Standardization of coverage APIs (coverage groups, bins, etc.)
  – Further explorations of needs regarding SystemC/TLM
UVM SystemC

• New standard under discussion in VWG
• Materializes the UVM methodology natively in SystemC
• Open source proof-of-concept implementation and LRM have been donated to Accellera
• Language Reference Manual under review/discussion right now
  – Please join us if you are interested!
Transaction Level Protocols PWG

• Proposed Charter
  
  **Provide a blueprint for the creation of SystemC Transaction Level Protocols, provide interoperable interfaces, develop best practices for SystemC interfaces and provide a process to ensure the timely delivery of those interfaces.**

• Proposed Scope
  – The working group will be narrowly focused on interfaces implemented in SystemC
  – We will not cover the existing TLM-2.0 ‘generic bus protocol’
  – The scope will be to define best practices and provide a procedure to ensure that interfaces are written to that standard
Transaction Level Protocols PWG – cont’d

• Proposed Goals
  – Establish a well-known location for SystemC Transaction Level Protocol (TLP) interfaces
  – Define and ensure TLP blueprint best practices as new TLP interfaces are standardized
  – Eliminate duplication of development effort and the necessity for adapters between divergent implementations of protocols
  – Establish timely process to incorporate contributions and feedback from wider open source community
  – Have the TLP blueprint used as the standard for interfaces developed outside the Accellera TLP working group (proprietary interfaces)

More info: [http://www.accellera.org/activities/proposed_working_groups](http://www.accellera.org/activities/proposed_working_groups)
Advancing Standards Together

• Share your experiences
  – Visit www.accellera.org and register to post on community forums at forums.accellera.org

• Show your support
  – Record your adoption of standards

• Become an Accellera member
  – Join working groups
Thank you!