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SystemC Synthesis Standard: Which Topics for Next Round?

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What to Standardize Next…

- Benefit of current standard:
  - Provides clear guidelines for synthesizability for C++/SystemC
  - Set clear subset for synthesis tools
- We are currently discussing the options for the next standard
- A big list of topics…
  - What is important to us designers?
  - What is valuable to EDA vendors?
  - What are the priorities?
  - Did we think of everything?

Join the discussion!
Join the SWG calls!

C++ Language and Math Libraries

- C++ / C++11
  - Unions
  - Constructor arguments
  - Automatic port naming VCD tracing for all ports for all ports
  - Safe array class
  - Type handling advances (auto, decl)
  - Many other features of interest …

- Math libraries
  - AC datatypes and SystemC datatypes
  - sc_complex
  - sc_float

Channel Libraries

- Which elements :
  - FIFOs
  - point-to-point
  - pulse
  - ring buffer
  - line buffers
  - CDC
  - etc.
- Standard interpretation of the TLM interface in synthesis
  - Must blocking vs. may-block vs. non-blocking
  - Use TLM 1.0 as reference or not (need add reset)

Micro-architecture Directives

- Standard list of directives :
  - Loop handling:
    - unroll, partial unroll, pipeline, sequential
  - Function handling
    - Sequential function, pipelined, parallel, map to custom resource, etc.
  - Array handling:
    - flatten, map-to-memory, map-to-reg-file, split, combine, resize, etc.
  - Custom resource:
    - pipelined, combinational
  - Inputs:
    - stable, delay
  - Latencies:
    - Min latency, max-latency
  - Etc.

Micro-architecture Directives

- How to specify the directives:
  - Pragma in the code
  - Tcl commands in synthesis directive file
  - Directive in code (empty functions or variables with specific meaning)

- How to apply the directives
  - How to “label” and “find” structures in the code
    - *“The loop filter_kernel, unroll it”*

Synthesis Structures

- How to interpret the SystemC CDFG and synthesis directive
  - The generated RTL behaves equivalently in all tools
  - Consistent interpretation across tools
- How to write a pipeline
  - Where to freeze, where to free the I/O
  - Where to expand the pipeline
- Cycle-accurate, cycle close and super-cycle modes
  - Clearly define and implement the scheduling mode
- How to specify and create custom resources
  - Specified as C++ functions or C++ scopes
  - What interfaces to they implement
  - Specify to characterize the custom resource or not with logic synthesis

Memories

- Where are the memories in the SystemC code:
  - Mapping of C++ array into memories (implicit)
  - Using memory channel (explicit)

- How to describe the memory macro to the HLS tool
  - Memory ports, timing, simulation model file, lib file, etc.
  - Standard format

- Using the memory macro in the design (architecture model)
  - Memory port sharing by more than one process in a module
  - Memory port sharing by sub-modules
  - Multi-clock memories
  - Memories inside or outside the module

Tools and Flows

- Standard interpretation of module hierarchy
  - How to set up project with submodules
    - Many modules and processes to synthesize, process them one by one or all at once
  - Where are the memories instantiated

- Standard minimal wrapper generation
  - Tool to provide wrapper for input SystemC in SystemVerilog context
  - Tool to provide wrapper for generated Verilog in SystemC

  - Mostly about datatype conversions
  - Make the wrapper lightweight enough so it can be used with various HDL simulators
  - Help ease flow migration

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Summary

- HLS is rapidly growing in adoption and proving its value for multiple users (design, verification, accelerated software…)
- Accellera SystemC synthesis subset standardization helps focus so the ecosystem can grow around it
- There are great areas for “what’s next” to standardize to complete the ecosystem for HLS

Join the discussion!
Join the SWG calls!
Drive what you need in the standard!

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Thank You!