Applying TLM 2.0 to Legacy Platforms

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Agenda

- Model Examples and Sources
- Example Legacy Platform
- How to fit in TLM-2.0 models
- Demonstration
MODEL EXAMPLES AND SOURCES
Finally: Model Interoperability

Previously proprietary (backdoor) APIs & new additions have now been standardized:

- **(DMI) Direct Memory Interface**
  - Direct backdoor access into memory
  - Allows un-inhibited ISS execution
- **LT (Loosely Timed) modeling**
  - Timing declaration
  - Allows speed/accuracy trade-offs
- **Temporal Decoupling**
  - Only synchronize when necessary
  - Allows multicore speedup
But: Challenging Choices

- 80+ MIPS
  - App View TLM (AV)
  - Pre-silicon Software Development & Integration

- 40-60 MIPS
  - Prog. View TLM (LT)

- 1-10 MIPS
  - Architectural Exploration & Real-Time SW Development
  - PV with Timing TLM (AT)

- 1-100 KIPS
  - C-translated-RTL Models
  - Co-Emulation
  - RTL co-simulation
  - System Verification

Functionally Accurate
Cycle Approximate
Cycle Accurate
But: Legacy causes more challenges

Each of the styles has several legacy predecessors which need to be connected

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Functionally Accurate

- C-translated-RTL Models
- Co-Emulation
- RTL co-simulation

Cycle Approximate

- Pre-silicon Software Development & Integration
- Architectural Exploration & Real-Time SW Development

Cycle Accurate

- System Verification
- App View TLM (AV)
- Prog. View TLM (LT)
- PV with Timing TLM (AT)
EXAMPLE LEGACY PLATFORM
A Portable Media Player
# Media Player Memory Map

**VPMP Virtual Platform**

For Synopsys Demo Platform

<table>
<thead>
<tr>
<th>Start Addr</th>
<th>End Addr</th>
<th>Component</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000000</td>
<td>0x000000FF</td>
<td>RAM - Vectors (4K)</td>
</tr>
<tr>
<td>0x01000000</td>
<td>0x010000FF</td>
<td>RAM - Code (8M)</td>
</tr>
<tr>
<td>0x02000000</td>
<td>0x020000FF</td>
<td>RAM - Stack (1M)</td>
</tr>
<tr>
<td>0x03000000</td>
<td>0x030000FF</td>
<td>RAM - Heap (16M)</td>
</tr>
<tr>
<td>0x08000000</td>
<td>0x080000FF</td>
<td>RAM - Spare</td>
</tr>
<tr>
<td>0x10000000</td>
<td>0x1001FFFF</td>
<td>DesignWare USB OTG</td>
</tr>
<tr>
<td>0x20000000</td>
<td>0x200000FF</td>
<td>UART</td>
</tr>
<tr>
<td>0x20010000</td>
<td>0x200100FF</td>
<td>Interrupt Controller</td>
</tr>
<tr>
<td>0x20004000</td>
<td>0x20004FFF</td>
<td>Core Manager</td>
</tr>
<tr>
<td>0x20010000</td>
<td>0x200100FF</td>
<td>Display Controller</td>
</tr>
<tr>
<td>0x20014000</td>
<td>0x20014FFF</td>
<td>MTool Interface</td>
</tr>
</tbody>
</table>

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HOW TO FIT IN TLM-2.0 MODELS
Legacy Platform - VPMP

- Models use legacy interfaces
  - Virtio VRE
  - Magic-C
Wrapping Process

For each legacy interface, a SystemC equivalent interface has been defined.

<table>
<thead>
<tr>
<th>Legacy Interface</th>
<th>SystemC Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td>iPin</td>
<td>pin_if&lt;int&gt;</td>
</tr>
<tr>
<td>iPIn2</td>
<td>pin2_if&lt;int, int&gt;</td>
</tr>
<tr>
<td>ILogger</td>
<td>pin_if&lt;float&gt;</td>
</tr>
<tr>
<td>iTrigger</td>
<td>trigger_if</td>
</tr>
<tr>
<td>iRegisterValues</td>
<td>register_values_if</td>
</tr>
<tr>
<td>iCoprocessor</td>
<td>coprocessor_if</td>
</tr>
<tr>
<td>iDisasm</td>
<td>disasm_if</td>
</tr>
</tbody>
</table>
Wrapping Process

- For the legacy memory transaction interface (iMemory) a TLM-2.0 compliant equivalent has been defined.

<table>
<thead>
<tr>
<th>Legacy Interface</th>
<th>SystemC Interface (TLM-2.0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>iMemory (initiator)</td>
<td><code>tlm::tlm_initiator_socket&lt;&gt;</code></td>
</tr>
<tr>
<td>iMemory (target)</td>
<td><code>tlm::tlm_target_socket&lt;&gt;</code></td>
</tr>
</tbody>
</table>
Wrapping Process

- Innovator Code Generator will automatically wrap the legacy interfaces with their SystemC equivalents when SystemC Build Option is selected.
Wrapping Process

• The SystemC code generated by Innovator for each wrapped model can be extracted to create a native SystemC component with TLM-2.0 memory transaction interfaces.
Innovator Wrapping Process

- Innovator also has the capability to import existing SystemC designs. As part of this process it creates a description file (.vsc) which determines how the model will appear in the Innovator IDE.
- We can use this process to create description files for the Innovator generated SystemC models.
Innovator Wrapping Process

• Using Innovators’ SystemC code generation and importing capability we have created a library of SystemC models – the DesignWare System Level Library.

• These can be used in any IEEE 1666 compliant environment including Innovator.

• All DW-SLL models have TLM-2.0 compliant transaction interfaces.
DesignWare System Level Library

Models from DesignWare System-Level library now have native TLM-2.0 interfaces.

- Example shown is USB OTG controller
- Uses Master and Slave TLM interfaces
- Directly reflects implementation register fields and parameters

DW-SLL Models can be used directly in Innovator projects. Can drag and drop these into existing designs.
DEMONSTRATION
Media Player Example & SystemC TLM 2.0
Media Player Example & SystemC TLM 2.0

To illustrate TLM-2.0 wrapping capability, we can import a native TLM-2.0 model from DW-SLL into the VPMP platform.

Existing design has a “wrapped” RAM model from which the program code is executed.

We can replace this with a native TLM-2.0 RAM from the DW-SLL and show that the system still executes code as expected.
First, we need to add DW-SLL as a library in Innovator

Right click on the “Libraries” folder and select “Add Library” from menu which results.

Fill in the Add Library dialog as follows. Set the path to point to the “generic” folder in DW-SLL.
Media Player Example & SystemC TLM 2.0

DW-SLL generic components are added as a library in Innovator.

Includes the SmartRam model we want to use in Innovator.

This can now be simply dragged and dropped into the design.
Media Player Example & SystemC TLM 2.0

Drag and drop “SmartRam” model into design alongside existing RAM model.

To connect the new model to the platform label its Memory “MainCode_Mem”.

The existing RAM model can then be deleted from the design.
Media Player Example & SystemC TLM 2.0

New “SmartRam” now has same connectivity and address mapping in the platform as the legacy RAM.

Can be seen that RAM model has TLM-2.0 target socket interface.

Now re-build the platform.
Media Player Example & SystemC TLM 2.0

The “Demo” program runs as before from the native TLM-2.0 RAM illustrating that the legacy platform has been correctly “wrapped” with TLM-2.0 memory transaction interfaces.
Summary

- Adapters necessary to connect to legacy
- Matching TLM philosophies important
- TLM-1.0 adapters exist

- TLM-2.0 Speed Results for proper use
  - DMI, LT modeling, Quantum
  - 3% to 10% speed degradation reported

- Vendors moving to TLM-2.0 fast
  - Example: Synopsys Innovator and DesignWare System-level Library are already fully TLM-2.0 compliant