Accellera Standards Update
UVM and IEEE-1800.2

On behalf of the working group
Srivatsa Vasudevan
srivats@synopsys.com
What is happening?
Deliverables

• IEEE 1800.2 WG
  – 1800.2 = SV focused
  – Defines UVM functional API (not an implementation)
  – Produces 1800.2 LRM
  – Allows for multiple implementations

• Accellera WG
  – Delivers UVM Library (SV) Reference Implementation matching 1800.2 LRM
  – Provide bug fixes for UVM library
Contribution options

- **IEEE 1800.2 WG**
  - For IEEE members every other week @ 9AM PST call
  - Tracking via accellera.mantishub.com → P1800.2

- **Accellera WG**
  - For Accellera members every other week @ 9AM PST call
  - Tracking via accellera.mantishub.com → UVM
General focus areas 1800.2

• Allow flexibility for future implementations
• Remove implementation artifacts from LRM
• Review API in the light of backward compatibility, consistency, simplification and extensibility
• Fully document and describe API

• (Note: Library can support deprecated API)
1800.2 REG Sub WG

- Identification and closure of register related issues
- Definition of necessary API to support future use models – e.g., SoC use models
- Further align reg sub system with other relevant standards (IP-XACT)
- Currently: Issue collection and prioritization
1800.2 TLM Sub WG

• Align UVM TLM with current IEEE 1666-2011 standardized TLM-1 and TLM-2.0 concepts
• Improve current UVM TLM standard documentation to explicitly explain execution semantics and underlying concepts
• Discuss completeness of current UVM TLM API
Thank You!